AMENDMENTS TO THE CLAIMS:

Claims 1, 10, 11 and 20 have been amended. Claim 26 has been added. No claims have been canceled. This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A method for etching a substrate, comprising:

providing a substrate having an aluminum oxide etch stop layer located thereunder;

providing a microelectronic device, the aluminum oxide etch stop layer positioned between the microelectronic device and substrate; and

etching an opening in said substrate using an etchant comprising a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of said carbon oxide is greater than about 80 sccm and said etchant is selective to said aluminum oxide etch stop layer, and without overetching said etch stop layer into said microelectronic device and without introducing hydrogen into the process.

2. (Original) The method as recited in Claim 1 wherein said flow rate of said carbon oxide ranges from about 150 sccm to about 220 sccm.

3. (Original) The method as recited in Claim 1 wherein said carbon oxide comprises carbon monoxide.

4. (Original) The method as recited in Claim 1 wherein said etch rate modulator comprises oxygen.

5. (Original) The method as recited in Claim 4 wherein a ratio of said fluorocarbon to said etch rate modulator is at least 2:1.

6. (Original) The method as recited in Claim 5 wherein a flow rate of said fluorocarbon ranges from about 12 sccm to about 18 sccm, and a flow rate of said etch rate modulator ranges from about 4 sccm to about 8 sccm.

7. (Original) The method as recited in Claim 1 wherein said etch rate modulator comprises nitrogen.

8. (Original) The method as recited in Claim 1 wherein said fluorocarbon comprises C_5F_8, C_4F_8, C_4F_6, C_2F_6, CF_4, NF_3, XeF_2, F_2, CHF_3, CH_2F_2, CH_3F, SF_6, or any combination thereof.

9. (Original) The method as recited in Claim 1 wherein said substrate is a dielectric material.

10. (Currently Amended) [[An]] <u>A</u> semiconductor device manufactured using the method for etching a substrate of Claim 1.

11. (Currently Amended) A method for manufacturing an integrated circuit, comprising:

providing semiconductor devices over a semiconductor substrate;

providing a dielectric layer over said semiconductor devices, said dielectric layer having an aluminum oxide etch stop layer located thereunder and without providing an additional barrier layer between the semiconductor devices and dielectric layer; and

etching openings in said dielectric layer using an etchant comprising a carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow rate of said carbon oxide is greater than about 80 sccm and said etchant is selective to said aluminum oxide etch stop layer; and

contacting said semiconductor devices through said openings.

12. (Original) The method as recited in Claim 11 wherein said flow rate of said carbon oxide ranges from about 150 sccm to about 220 sccm.

13. (Original) The method as recited in Claim 11 wherein said carbon oxide comprises carbon monoxide.

14. (Original) The method as recited in Claim 11 wherein said etch rate modulator comprises oxygen.

15. (Original) The method as recited in Claim 14 wherein a ratio of said fluorocarbon to said etch rate modulator is at least 2:1.

16. (Original) The method as recited in Claim 15 wherein a flow rate of said fluorocarbon ranges from about 12 sccm to about 18 sccm, and a flow rate of said etch rate modulator ranges from about 4 sccm to about 8 sccm.

17. (Original) The method as recited in Claim 11 wherein said etch rate modulator comprises nitrogen.

18. (Original) The method as recited in Claim 11 wherein said fluorocarbon comprises C_5F_8, C_4F_8, C_4F_6, C_2F_6, CF_4, NF_3, XeF_2, F_2, CHF_3, CH_2F_2, CH_3F, SF_6, or any combination thereof.

19. (Original) The method as recited in Claim 11 wherein at least one of said semiconductor devices is a ferroelectric capacitor.

20. (Currently Amended) An integrated circuit manufactured using the method, comprising:

providing semiconductor devices over a semiconductor substrate;

providing a dielectric layer over said semiconductor devices, said dielectric layer having an aluminum oxide etch stop layer located thereunder <u>and without providing an additional barrier layer between the semiconductor devices and dielectric layer</u>; and

etching openings in said dielectric layer using an etchant comprising carbon oxide, a fluorocarbon, an etch rate modulator, and an inert carrier gas, wherein a flow

rate of said carbon oxide is greater than about 80 sccm and said etchant is selective to said aluminum oxide etch stop layer; and

contacting said semiconductor devices through said openings.

21. (Original) The integrated circuit as recited in Claim 20 wherein at least one of said semiconductor devices is a ferroelectric capacitor.

22. (Withdrawn) An integrated circuit, comprising:

semiconductor devices located over a semiconductor substrate;

a dielectric layer located over said semiconductor devices, said dielectric layer having an aluminum oxide etch stop layer located thereunder; and

interconnects located in said dielectric layer and in contact with said aluminum oxide etch stop layer, said interconnects contacting said semiconductor devices thereby forming an operative integrated circuit.

23. (Withdrawn) The integrated circuit as recited in Claim 22 wherein said dielectric layer and said aluminum oxide etch stop layer are located in a back-end of line of said integrated circuit.

24. (Withdrawn) The integrated circuit as recited in Claim 22 wherein said dielectric layer is a first dielectric layer and said aluminum oxide etch stop layer is a first aluminum oxide etch stop layer, and further including multiple other dielectric layers and

aluminum oxide etch stop layers located over said first dielectric layer and said first aluminum oxide etch stop layer.

25. (Withdrawn) The integrated circuit as recited in Claim 24 being void of silicon nitride etch stop layers.

26. (New) The method as recited in Claim 1 wherein the method is without providing an additional barrier layer between the microelectronic device and substrate.